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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/979,587	11/26/2001	Kuniyuki Kajita	L9289.01217	3448

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EXAMINER	
TALAPATRA, ANIKA F	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/979,587	KAJITA, KUNIYUKI	
	Examiner	Art Unit	
	Anika F. Talapatra	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/979,587.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *24May2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 26 November 2001 was filed after the mailing date of the 26 November. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 to 14 rejected under 35 U.S.C. 102(b) as being anticipated by Shiino et al. (US. Patent 5964607) (hereafter referred to as Shiino).

As to claim 1, Shiino teaches a gain control apparatus comprising: an average power calculator (figure 3, 46), a direct current (DC) offset detector (figure 3, 58), a gain value determining means (figure 3, 50, 52, 54, 56, Vagc), and a gain-controllable amplifier (figure 3, 40). The output of the average power calculator as taught by Shiino (column 4 line 63- column 5 line 9) is compared to a reference power generator, to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation. The DC offset detector as taught by

Shiino (column 4 line 63- column 5 line 2) is functionally equivalent to the difference detecting means as claimed by the applicant. The DC offset detector calculates a difference between the received signal and a reference value. The gain value determining means as taught by Shiino (column 5, lines 3-33) is functionally equivalent to a voltage control value calculating means as claimed by the applicant. The gain value determining means outputs a value that is used to amplify the received signal. The gain-controllable amplifier as taught by Shiino (column 4, lines 43-51, column 6 lines 11-28) is functionally equivalent to an amplifying means as claimed by the applicant. The gain-controllable amplifier amplifies the received signal by a calculated value output from the gain value determining means.

As to claim 2, Shiino teaches the output of the average power calculator (column 4 line 63- column 5 line 9, figure 3, CLd(n), 46) is compared to a reference power generator (figure 3, CLr), to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation.

As to claim 3, Shiino teaches an analog to digital (A/D) converter (figure 3, 42) for performing digital conversion of the received signal. Shiino teaches the output of the A/D converter as input to an average power calculator, after the DC offset set was removed from the signal. Shiino teaches the output of the average power calculator (column 4 line 63- column 5 line 9, figure 3 CLd(n), 46) is compared to a reference power generator (figure 3 CLr), to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant.

As to claim 4, Shiino teaches average power level calculation of the input signal (column 4 line 63- column 5 line 9, figure 3, CLd(n), 46) this average is compared to a reference, or preset value, the power generator level (figure 3, CLr), to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation.

As to claim 5, Shiino teaches the average power calculator, calculates the average power of the input signal, (column 4 line 63- column 5 line 9, figure 3, CLd(n)) is compared to a reference, the power generator level (figure 3, CLr), to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation.

As to claim 6, Shiino teaches the average power calculator, calculates the average power of the input signal, (column 4 line 63- column 5 line 9, figure 3, CLd(n)) this average is compared to a reference, the power generator level (figure 3, CLr), to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation.

As to claim 7, Shiino teaches the gain value determining means, (column 5, lines 3-33, figure 3, 50, 90, 52, 56) is functionally equivalent to a voltage control value calculating means as claimed by the applicant. The gain value determining means outputs a value that is used to amplify the received signal. The gain-controllable amplifier as taught by Shiino (column 4, lines 43-51, figure 3, Vagc, 40) is functionally equivalent to an amplifying means as claimed by the applicant. The gain-controllable amplifier amplifies the received signal by a calculated value output from the gain value determining means, Vagc.

As to claim 8, Shiino teaches the average power calculator, calculates the average power of the input signal (column 4 line 63- column 5 line 9, figure 3, CLd(n)). Calculating the average power of the input signal, as taught by Shiino, is functionally equivalent to calculating the square of the average of both the in-phase and quadrature phase components of the input signal, and adding these two averages, as claimed by the applicant.

As to claim 9, Shiino teaches the average power calculator, calculates the average power of the input signal (column 4 line 63- column 5 line 9, figure 3, CLd(n)). Calculating the average power of the input signal, as taught by Shiino, is functionally

equivalent to calculating an average value obtained by squaring both the in-phase and quadrature phase components of the input signal, as claimed by the applicant.

As to claim 10, Shiino teaches the average power calculator, calculates the average power of the input signal (column 4 line 63- column 5 line 9, figure 3, CLd(n)). Calculating the average power of the input signal is calculated for each value r(n), n = 0, 1, 2, ..., where r(n) is the digitized input signal.

As to claim 11, Shiino teaches the average power calculator, calculates the average power of the input signal (column 4 line 63- column 5 line 9, figure 3, CLd(n)). Calculating the average power of the input signal is calculated for each value r(n), n = 0, 1, 2, ..., where r(n) is the digitized input signal. The signal Cr(n) is held constant by the automatic gain control apparatus (column 6 lines 11-28, figure 3, 36).

As to claim 12, Shiino teaches a communication terminal apparatus (column 4, lines 23-52) with a gain control apparatus comprising: an average power calculator (figure 3, 46), a DC offset detector (figure 3, 58), a gain value determining means (figure 3, 50, 52, 54, 56, Vagc), and a gain-controllable amplifier (figure 3, 40). The output of the average power calculator as taught by Shiino (column 4 line 63- column 5 line 9) is compared to a reference power generator, to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation. The DC offset detector as taught by Shiino (column 4 line 63- column 5 line 2) is functionally equivalent to difference detecting means as claimed by the applicant. The DC offset detector calculates a difference between the received signal and a reference value. The gain value determining means as taught by Shiino (column 5, lines 3-19) is functionally equivalent to a voltage control value calculating means as claimed by the applicant. The gain value determining means outputs a value that is used to amplify the received signal. The gain-controllable amplifier as taught by Shiino (column 4, lines 43-51) is functionally equivalent to an amplifying means as claimed by the applicant. The gain-controllable amplifier amplifies the received signal by a calculated value output from the gain value determining means.

As to claim 13, Shiino teaches a base station apparatus (column 4, lines 23-52) with a gain control apparatus comprising: an average power calculator (figure 3, 46), a DC offset detector (figure 3, 58), a gain value determining means (figure 3, 50, 52, 54, 56, Vagc), and a gain-controllable amplifier (figure 3, 40). The output of the average power calculator as taught by Shiino (column 4 line 63- column 5 line 9) is compared to a reference power generator, to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation. The DC offset detector as taught by Shiino (column 4 line 63- column 5 line 2) is functionally equivalent to the difference detecting means as claimed by the applicant. The DC offset detector calculates a difference between the received signal and a reference value. The gain value determining means as taught by Shiino (column 5, lines 3-33) is functionally equivalent to a voltage control value calculating means as claimed by the applicant. The gain value determining means outputs a value that is used to amplify the received signal. The gain-controllable amplifier as taught by Shiino (column 4, lines 43-51, column 6 lines 11-28) is functionally equivalent to an amplifying means as claimed by the applicant. The gain-controllable amplifier amplifies the received signal by a calculated value output from the gain value determining means.

As to claim 14, Shiino teaches a method and apparatus for gain control comprising: an average power calculator (figure 3, 46), a DC offset detector (figure 3, 58), a gain value determining means (figure 3, 50, 52, 54, 56, Vagc), and a gain-controllable amplifier (figure 3, 40). The output of the average power calculator as taught by Shiino (column 4 line 63- column 5 line 9) is compared to a reference power generator, to produce an output ΔL; ΔL is functionally equivalent to the convergence coefficient output from the convergence coefficient determining means as claimed by the applicant. ΔL is used in voltage control value calculation. The DC offset detector as taught by Shiino (column 4 line 63- column 5 line 2) is functionally equivalent to the difference detecting means as claimed by the applicant. The DC offset detector calculates a difference between the received signal and a reference value. The gain value determining means as taught by Shiino (column 5, lines 3-33) is functionally equivalent

to a voltage control value calculating means as claimed by the applicant. The gain value determining means outputs a value that is used to amplify the received signal. The gain-controllable amplifier as taught by Shiino (column 4, lines 43-51, column 6 lines 11-28) is functionally equivalent to an amplifying means as claimed by the applicant. The gain-controllable amplifier amplifies the received signal by a calculated value output from the gain value determining means.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

i. U.S. Patent 5432794, Yaguchi;

ii. U.S. Patent 6321073, Luz et al.; and

iii. U.S. Patent 5422606, Tanaka.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anika F. Talapatra whose telephone number is 571-272-6039. The examiner can normally be reached on 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. T.

KEVIN BURD
PRIMARY EXAMINER